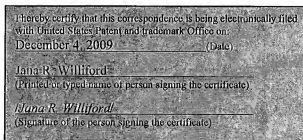


## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant: Simon Knowles  
Serial No.: 10/813,615  
Filed: 03/31/2004  
Title: APPARATUS AND METHOD FOR ASYMMETRIC  
DUAL PATH PROCESSING  
Grp./A.U.: 2183  
Examiner: Robert E. Fennema  
Confirmation No.: 3818

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450



Sir:

**PRE-APPEAL BRIEF REQUEST FOR REVIEW**

The Appellant has carefully considered this application in connection with the Final Rejection of August 4, 2009, the Advisory Action of October 22, 2009, and the telephonic interview of December 2, 2009. The Appellant respectfully requests a pre-appeal review of this application in view of the following remarks that reflect and include the substance of the telephonic interview.

### REMARKS/ARGUMENTS

The Appellant originally submitted Claims 1-21 in the application. In previous responses, the Appellant amended Claims 1-3, 5-6, 8, 11, 14-16, 18, and 21 and cancelled Claims 7 and 19-20 without prejudice or disclaimer. The previous amendment, which the Examiner noted would be entered for an appeal, included a correction of a typographical error in Claim 21. Claims 1-6, 8-18 and 21 are currently pending in the application.

#### **I. Rejection of Claims 1-7, 11, 14-18 and 21 under 35 U.S.C. §103**

The Examiner has rejected Claims 1-7, 11, 14-18 and 21 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,922,065 to Hull ("Hull"), in view of an article entitled, "Unifying FPGAs and SIMD Arrays" by Bolotski, *et al.* ("Bolotski") and further in view of an article entitled, "Computer Architecture: A Quantitative Approach" by Hennessy ("Hennessy"). The Appellant respectfully disagrees as argued below.

The Examiner appears to rely on the template field of Hull to disclose decoding identification bits of each instruction packet to determine which type of instruction packet is being decoded. (*See* Final Rejection, page 4, referring to column 3, lines 63-66, of Hull.) The template field of Hull, however, is used for mapping instruction slots to execution type units. (*See* column 3, lines 65-66.) An instruction slot is not an instruction packet as presently claimed but instead is part of an instruction bundle that includes multiple instruction slots. (*See* column 3, lines 52-60 and FIG. 3.) Thus, instead of determining which type of instruction packet is being decoded as recited in Claim 1, Hull is concerned with the individual instructions in a bundle and mapping the individual instructions to specific execution units. Hull, therefore, operates with a different architecture that does not appear to be concerned with which channel to send an instruction packet for processing but with what execution unit to send an instruction from an instruction slot. As such, Hull does not teach or suggest each element for which it has been cited. Neither Bolotski nor Hennessy have been cited to cure the above noted deficiency of Hull but to address other deficiencies of Hull noticed by the Examiner. As such, the applied combination of Hull, Bolotski and Hennessy does not teach or suggest each element of independent Claim 1 and Claims dependent thereon. Similarly, the applied

combination does not teach or suggest each element of independent Claims 18 and 21 and Claims dependent thereon.

The combination of Hennessy with Hull is also improper. The Examiner asserts that Hull “does not teach a variable-length instruction set, and thus, cannot teach a control instruction with a bit-width shorter than a data processing instruction.” (See Final Rejection, page 15, point 21.) The Examiner applies Hennessy to teach there are different ways to teach an instruction set (variable, fixed or a hybrid of the two) and each way has advantages or disadvantages. (See Final Rejection, page 16, point 21.)

The Appellant fails to find, however, why one skilled in the art would be motivated to apply the asserted teachings of Hull to a variable-length instruction set as asserted by the Examiner. (See, for example, the Advisory Action.) On the contrary, Hull is directed to reducing waste and inefficiency in encoding associated with fixed formats. (See column 2, lines 3-8, and column 5, lines 5-8.) Hull discloses using a template field to specify group boundaries within a bundle and the mapping of instruction slots to execution unit types. (See, for example, column 4, lines 20-26 and FIG. 4.) One skilled in the art, however, would not be motivated to employ the teachings of Hull in a variable-length format since a variable-length format would not have the waste and inefficiency of encoding that Hull addresses. In other words, Hull addresses problems associated with a fixed-length format. As such, one skilled in the art would not find Hull beneficial for a variable-length architecture. Accordingly, the combination of Hennessy with Hull is improper.

Additionally, since Hull is for fixed-length formats and the combination of Hennessy with Hull is improper, as argued in the previous response, the applied combination also fails to teach or suggest “control instructions having a control bit width” and “data processing instructions having a data processing bit width wider than the control bit width” as recited in Claim 1.

Thus, for at least the above reasons, the applied combination of Hull, Bolotski and Hennessy does not provide a *prima facie* case of obviousness of independent Claim 1 and Claims dependent thereon. Similarly, the applied combination does not provide a *prima facie* case of obviousness of independent Claims 18 and 21 and Claims dependent thereon. The Appellant therefore respectfully requests the Reviewers to reverse the Final Rejection of Claims 1-7, 11, 14-18 and 21 and allow issuance thereof.

The above arguments notwithstanding Claim 1 is not obvious in view of the cited prior art for the following reasons, also.

As the Examiner states, Hennessy discloses variable length instructions. Figure D.8 on page D-13 in Hennessy shows different instructions having different lengths. However, Hennessy does not appear to refer to instruction packets comprising a plurality of instructions of different lengths. The 'bundles' (30) shown in Figure 3 of Hull contain three 41-bit instruction slots, a 4-bit template field and a stop bit. The template field specifies the mapping of instruction slots to execution unit types. As stated in column 3, lines 61 to 63 all instructions in the instruction set of the processor are 41 bits in length.

Neither Hull nor Hennessy disclose instruction packets comprising different types of instructions having different bit lengths, whilst the instruction packets all have equal bit lengths. Using variable length instructions in the system of Hull would result in variable length instruction packets, *i.e.*, the instruction packets would not all have equal bit lengths.

It is therefore submitted that none of the cited prior art documents in combination or otherwise disclose or suggest the combination of features in Claim 1 including: "instruction packets comprising a plurality of only control instructions, the control instructions having a control bit width," "instructions packets comprising a plurality of instructions comprising at least one data processing instruction, the data processing instructions having a data processing bit width wider than the control bit width" and "the instruction packets being all of equal bit length." For at least this reason it is submitted that Claim 1 is not obvious in view of the cited prior art documents.

Furthermore, Claim 1 now explicitly states that the decode unit passes control instructions having the control bit width to a control processing channel and passes data processing instructions having the data processing bit width wider than the control bit width to a data processing channel. The cited prior art appears to fail to disclose or suggest to pass instructions of different bit widths to different processing channels. This novel feature advantageously allows the different channels to be adapted and optimized to handling instructions of different sizes. For at least this reason it is submitted that Claim 1 is not obvious in view of the cited prior art documents.

### III. Rejection of Claims 8-10, 12 and 13 under 35 U.S.C. §103

The Examiner has rejected Claims 8-10, 12, and 13 under 35 U.S.C. §103(a) as being unpatentable over Hull, Hennessy, and Bolotski in further view of *In re Rose*. As noted above, the cited combination of Hull, Hennessy and Bolotski does not provide a *prima facie* case of obviousness of independent Claim 1. *In re Rose* has not been cited to cure the above noted deficiencies of Hull, Hennessy and Bolotski but to address the additional limitations of dependent Claims 8-10, 12 and 13. The cited combination of Hull, Hennessy, Bolotski and *In re Rose*, therefore, does not provide a *prima facie* case of obviousness of independent Claim 1 and Claims 8-10, 12 and 13 which depend thereon. The Appellant, therefore, respectfully requests the Reviewers to reverse the Final Rejection of Claims 8-10, 12 and 13 and allow issuance thereof.

### IV. Conclusion

In view of the foregoing remarks, the Appellant sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-6, 8-18 and 21.

The Appellant requests the Reviewers to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

HITT GAINES, PC

/J. Joel Justiss/

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Registration No. 48,981

Dated: December 4, 2009  
P.O. Box 832570  
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**PRE-APPEAL BRIEF REQUEST FOR REVIEW**

Docket Number (Optional)

ICER-321547

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on December 4, 2009

Signature /Jana R. Williford/Typed or printed name Jana R. Williford

Application Number

10/813,615

Filed

2004-03-31

First Named Inventor

Simon Knowles

Art Unit

2183

Examiner

Robert E. Fennema

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.
/J. Joel Justiss/
☐ assignee of record of the entire interest.  
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.  
(Form PTO/SB/96)

Signature

J. Joel Justiss

Typed or printed name

☒ attorney or agent of record.  
Registration number 48,981
972-480-8800

Telephone number

☐ attorney or agent acting under 37 CFR 1.34.
December 4, 2009

Registration number if acting under 37 CFR 1.34 \_\_\_\_\_

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required.  
Submit multiple forms if more than one signature is required, see below.

☒ \*Total of 1 forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.